\*\*\*\*\*\* PlanAhead v14.7 (64-bit)

\*\*\*\* Build 321239 by xbuild on Fri Sep 27 19:29:51 MDT 2013

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INFO: [Common 17-78] Attempting to get a license: PlanAhead

INFO: [Common 17-290] Got license for PlanAhead

INFO: [Device 21-36] Loading parts and site information from C:/Xilinx/14.7/ISE\_DS/PlanAhead/data/parts/arch.xml

Parsing RTL primitives file [C:/Xilinx/14.7/ISE\_DS/PlanAhead/data/parts/xilinx/rtl/prims/rtl\_prims.xml]

Finished parsing RTL primitives file [C:/Xilinx/14.7/ISE\_DS/PlanAhead/data/parts/xilinx/rtl/prims/rtl\_prims.xml]

start\_gui

source C:/Users/projpc1/Desktop/Lab3/pa.fromHdl.tcl

# create\_project -name Lab3 -dir "C:/Users/projpc1/Desktop/Lab3/planAhead\_run\_4" -part xc3s500eft256-4

# set\_param project.pinAheadLayout yes

# set srcset [get\_property srcset [current\_run -impl]]

# set\_property target\_constrs\_file "nbit\_twisted\_ring\_counter.ucf" [current\_fileset -constrset]

Adding file 'C:/Users/projpc1/Desktop/Lab3/nbit\_twisted\_ring\_counter.ucf' to fileset 'constrs\_1'

# set hdlfile [add\_files [list {D\_flipflop.vhd}]]

# set\_property file\_type VHDL $hdlfile

# set\_property library work $hdlfile

# set hdlfile [add\_files [list {nbit\_reg.vhd}]]

# set\_property file\_type VHDL $hdlfile

# set\_property library work $hdlfile

# set hdlfile [add\_files [list {not\_gate.vhd}]]

# set\_property file\_type VHDL $hdlfile

# set\_property library work $hdlfile

# set hdlfile [add\_files [list {nbit\_shiftreg.vhd}]]

# set\_property file\_type VHDL $hdlfile

# set\_property library work $hdlfile

# set hdlfile [add\_files [list {nbit\_twisted\_ring\_counter.vhd}]]

# set\_property file\_type VHDL $hdlfile

# set\_property library work $hdlfile

# set\_property top nbit\_twisted\_ring\_counter $srcset

# add\_files [list {nbit\_twisted\_ring\_counter.ucf}] -fileset [get\_property constrset [current\_run]]

# open\_rtl\_design -part xc3s500eft256-4

Using Verific elaboration

Parsing VHDL file "C:/Xilinx/14.7/ISE\_DS/PlanAhead/data/parts/xilinx/rtl/lib/synplify/synattr.vhd" into library synplify

Parsing VHDL file "C:/Xilinx/14.7/ISE\_DS/PlanAhead/data/parts/xilinx/rtl/lib/synplify/synattr.vhd" into library synplify

Parsing VHDL file "C:/Users/projpc1/Desktop/Lab3/D\_flipflop.vhd" into library work

Parsing VHDL file "C:/Users/projpc1/Desktop/Lab3/nbit\_reg.vhd" into library work

Parsing VHDL file "C:/Users/projpc1/Desktop/Lab3/not\_gate.vhd" into library work

Parsing VHDL file "C:/Users/projpc1/Desktop/Lab3/nbit\_shiftreg.vhd" into library work

Parsing VHDL file "C:/Users/projpc1/Desktop/Lab3/nbit\_twisted\_ring\_counter.vhd" into library work

INFO: [Designutils 20-910] Reading macro library C:/Xilinx/14.7/ISE\_DS/PlanAhead/data\./parts/xilinx/spartan3e/spartan3e/hd\_int\_macros.edn

Parsing EDIF File [C:/Xilinx/14.7/ISE\_DS/PlanAhead/data\./parts/xilinx/spartan3e/spartan3e/hd\_int\_macros.edn]

Finished Parsing EDIF File [C:/Xilinx/14.7/ISE\_DS/PlanAhead/data\./parts/xilinx/spartan3e/spartan3e/hd\_int\_macros.edn]

Loading clock regions from C:/Xilinx/14.7/ISE\_DS/PlanAhead/data\parts/xilinx/spartan3e/spartan3e/xc3s500e/ClockRegion.xml

Loading clock buffers from C:/Xilinx/14.7/ISE\_DS/PlanAhead/data\parts/xilinx/spartan3e/spartan3e/xc3s500e/ClockBuffers.xml

Loading package from C:/Xilinx/14.7/ISE\_DS/PlanAhead/data\parts/xilinx/spartan3e/spartan3e/xc3s500e/ft256/Package.xml

Loading io standards from C:/Xilinx/14.7/ISE\_DS/PlanAhead/data\./parts/xilinx/spartan3e/IOStandards.xml

INFO: [Device 21-19] Loading pkg sso from C:/Xilinx/14.7/ISE\_DS/PlanAhead/data\parts/xilinx/spartan3e/spartan3e/xc3s500e/ft256/SSORules.xml

Loading list of drcs for the architecture : C:/Xilinx/14.7/ISE\_DS/PlanAhead/data\./parts/xilinx/spartan3e/spartan3e/drc.xml

INFO: [Timing 38-77] Reading timing library C:/Xilinx/14.7/ISE\_DS/PlanAhead/data\parts/xilinx/spartan3e/spartan3e/spartan3e-4.lib.

INFO: [Timing 38-34] Done reading timing library C:/Xilinx/14.7/ISE\_DS/PlanAhead/data\parts/xilinx/spartan3e/spartan3e/spartan3e-4.lib.

Parsing UCF File [C:/Users/projpc1/Desktop/Lab3/nbit\_twisted\_ring\_counter.ucf]

Finished Parsing UCF File [C:/Users/projpc1/Desktop/Lab3/nbit\_twisted\_ring\_counter.ucf]

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

Phase 0 | Netlist Checksum: 7dff5575

update\_compile\_order -fileset sim\_1

startgroup

set\_property package\_pin C11 [get\_ports {Q\_outputs[0]}]

endgroup

startgroup

set\_property package\_pin D11 [get\_ports {Q\_outputs[1]}]

endgroup

startgroup

set\_property package\_pin B11 [get\_ports {Q\_outputs[2]}]

endgroup

startgroup

set\_property package\_pin A12 [get\_ports {Q\_outputs[3]}]

endgroup

startgroup

set\_property package\_pin A13 [get\_ports {Q\_outputs[4]}]

endgroup

startgroup

set\_property package\_pin B13 [get\_ports {Q\_outputs[5]}]

endgroup

startgroup

set\_property package\_pin A14 [get\_ports {Q\_outputs[6]}]

endgroup

startgroup

set\_property package\_pin B14 [get\_ports {Q\_outputs[7]}]

endgroup

startgroup

set\_property package\_pin D12 [get\_ports reset]

endgroup

startgroup

set\_property package\_pin C12 [get\_ports preset]

endgroup

set\_property package\_pin "" [get\_ports [list CLK]]

save\_constraints

exit

ERROR: [Common 17-39] 'stop\_gui' failed due to earlier errors.

INFO: [Common 17-206] Exiting PlanAhead at Thu Nov 02 11:12:52 2017...

INFO: [Common 17-83] Releasing license: PlanAhead